Study of Self-Heating Effects, Temperature-Dependent Modeling, and Pulsed Load–Pull Measurements on GaN HEMTs

Sebastien Nuttinck, Edward Gebara, Joy Laskar, *Member, IEEE*, and Herbert M. Harris, *Senior Member, IEEE*

***Abstract*—On-wafer RF and *IV* characterizations are performed for the first time on power GaN high electron-mobility transistors (HEMTs) under pulse and continuous conditions at different temperatures. These measurements give an in-depth understanding of self-heating effects and allow one to investigate the possibility of improving heat-dissipation mechanisms. A pulsed load–pull system that measures the power gain of the device-under-test (DUT) under pulsed RF and bias condition has been developed. To the best of our knowledge, this is the first time that the reflected power at the DUT is measured under the pulse mode of operation. Additionally, an improved small-signal model for power GaN HEMTs that incorporates the geometry of the device is developed at various temperatures. This is the basis for empirical large-signal modeling.**

***Index Terms*—GaN HEMTs, microwave power FETs, modeling, pulsed load–pull, self-heating effects.**

I. Introduction

THE wireless communication market is growing rapidly and there is a great demand for high-power transistors for applications such as phased-array antennas and base stations. Today, available power transistors are in the 1-W/mm range. Candidates to fill the need for higher output power are Si-LDMOS and SiC/GaN-based transistors. They offer power densities in the few watts per millimeter range because of their high breakdown voltage [1]–[7]. GaN-based compared to SiC-based transistors and Si-LDMOS offers higher cutoff frequencies and maximum frequencies of oscillation ($f_{\mathrm{T}} \approx 25$ GHz, and $f_{\mathrm{MAX}} \approx 33$ GHz) [2], [4], [5].

Pulsed RF and bias measurement systems have been developed to overcome self-heating effects that perturb measurements performed with traditional continuous characterization systems. Such systems allow one to understand the ideal characteristics of a device, and build accurate models for applications that work under a pulsed mode of operation such as time-division multiple access (TDMA). The study of power devices under pulsed conditions and under different temperatures of operation allows one to understand the thermal behavior and to answer the question of whether or not improvements in heat sinks will ameliorate the device's characteristics. Additionally, studying devices under these conditions enables one to build more robust models that help understand the device physics [6], [8]–[10].

The design of RF circuits requires reliable and accurate nonlinear models. During the past 15 years, most of the work in the RF nonlinear modeling area has essentially been focused on GaAs MESFETs/high electron-mobility transistors (HEMTs), and Si MOSFETs [11], [12]. Improvements in the models have progressively been made to predict more accurately the fundamental frequency, as well as harmonics and intermodulation distortion at different bias conditions, temperatures, and terminations. As a result, nonlinear empirical models incorporate a large number of fitting parameters and external circuit elements [11]. RF nonlinear modeling methods of GaN HEMTs can be derived from techniques applied to GaAs and Si FETs.

In this paper, we present on-wafer measurement results featuring *IV*, S-parameters, and load–pull characteristics at different temperatures. Both *IV* and RF power characteristics are achieved in continuous and pulsed modes. Additionally a small-signal model that operates up to 15 GHz has been extracted for different bias conditions and at various temperatures of operation, enabling large-signal transistor modeling.

This paper is organized as follows. Section II presents details of the measurement techniques. Section III shows the study of self-heating effects through dc/pulsed *IV* and small-signal RF characterization with the temperature of operation as an additional parameter. Modeling of GaN HEMTs for different temperatures is presented in Section IV. The results of cryogenic load–pull measurements are presented in Section V. Section VI presents a conclusion.

II. Experimental Setup

On-wafer measurements have been carried out at temperatures as low as 65 K using a custom-made cryogenic probe station. The cryogenic probing system (Fig. 1) contains ports for RF and dc cables, temperature sensors, vacuum pumps, coplanar waveguide probes with manipulators, and a closed-cycle helium refrigerator cold head. The device-under-test (DUT) is mounted

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S. Nuttinck and J. Laskar are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

E. Gebara is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA and is also with Quellan Inc., Atlanta, GA 30318 USA.

H. M. Harris is with the Electro-Optics Environment and Materials Laboratory, Georgia Tech Research Institute, Atlanta, GA 30332 USA.

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Fig. 1. Photography of the cryogenic microwave probe station.

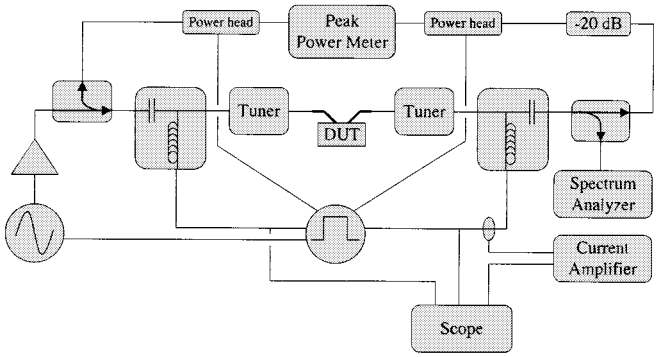


Fig. 2. Schematic of the measurement system.

on the cold wafer stage and the test chamber is evacuated to prevent frost buildup and large thermal gradients when cooling the chamber.

The experimental setup consists of two pulse bias generators, a frequency source synchronized with the pulse generators, a solid-state power amplifier, and mechanical tuners to control the load and source impedances at the DUT. The current is monitored with a digitizing scope through a current probe. The RF power is monitored with a peak power meter. Measurements are achieved at a gate baseline that is in the pinchoff region of the DUT. Both the drain and RF pulsewidth are shorter and delayed by a few 100 ns in order to be centered in the gate pulse. Fig. 2 presents a diagram of the setup used.

An S-parameter calibration of all elements (fixtures, bias tees, couplers, cables, adapters, etc.) is used to retrieve the actual power at the input and output of the DUT. To our knowledge, we are the first to measure the reflected power under pulsed conditions and under a large-signal mode of operation for various load and source impedances (load–pull measurement setup), allowing us to extract the power gain ($G_{\rm P}$) of the DUT in addition to the transducer gain ($G_{\rm T}$).

The studied GaN HEMTs are provided by CREE Inc., Durham, NC, and are grown on an SiC substrate, with a gatewidth of 125 μm per finger. Measurements were performed on different devices with various gate lengths ($L_{\rm G}$), number of fingers, gate-to-source lengths ($L_{\rm GS}$), and gate-to-drain lengths ($L_{\rm GD}$).

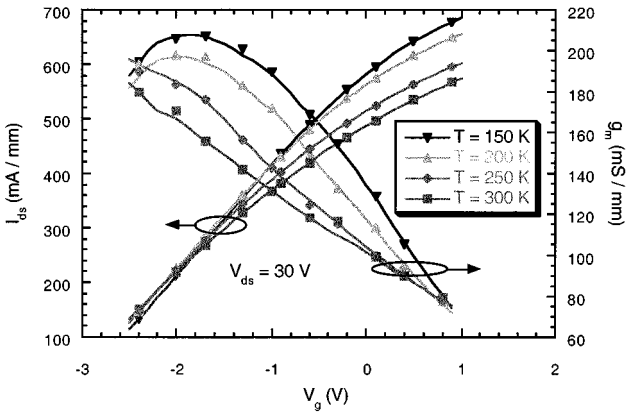


Fig. 3. Transconductance and drain current versus $V_{\rm GS}$ for various temperatures at $V_{\rm DS} = 30$ V.

III. Study of Self-Heating Effects Through DC/Pulsed *IV* and Small-Signal RF Characterization at Various Temperatures

Under large drain bias, the device lattice temperature increases and so does the carrier phonon scattering rate, which leads to a drop in the carrier mobility. This effect has been reported to be of great influence in reducing the output conductance of FETs [13], and is commonly referred as "self-heating." Evidence of such an effect is a negative slope in $I_{\rm DS}(V_{\rm DS})$. Biasing devices during a short period of time reduces carrier/lattice exchanges and, therefore, one can control the heat dissipation in the device. Experiments performed using pulsed *IV* systems support this assumption by showing characteristics free of self-heating [14]–[16].

The lattice temperature is also well known to be of significant influence on the carrier mobility and, therefore, on the device characteristics.

In this section, we present a study of heating effects in GaN HEMTs through dc/pulsed *IV* and small-signal RF characterization at various temperatures of operation.

A. DC/Pulsed IV Characterization

The GaN HEMT dc characteristics show an increase in the drain current and device transconductance while operating at a reduced temperature (Fig. 3). The improvements are results of an increase in electron mobility [17].

Fig. 4 exhibits pulsed *IV* measurement characteristics at 300 K for various duty cycle at 0-V gate bias and a pulse period of 100 μs. By gradually reducing the pulsewidth, the negative slope of the $I_{\rm DS}(V_{\rm DS})$ characteristics diminishes.

Fig. 5 compares the drain-to-source current at 300 and 65 K under a pulsed and continuous mode of operation. Pulsed characteristics are obtained with a signal period of 100 μs, and a pulsewidth of 1 μs on the drain side. Unlike at 300 K, pulsed and continuous *IV* characteristics at $T = 65$ K correlate for drain voltages larger than 15 V. The mismatch observed at 65 K at low drain voltages has been reported in [18].

Fig. 6 shows the temperature effects on dc–$I_{\rm DS}(V_{\rm DS})$ and dc–$I_{\rm GS}(V_{\rm DS})$ characteristics. At any temperature, it is possible to define the drain voltage threshold as the drain voltage value at which the drain current starts to decrease. It is noteworthy that, as

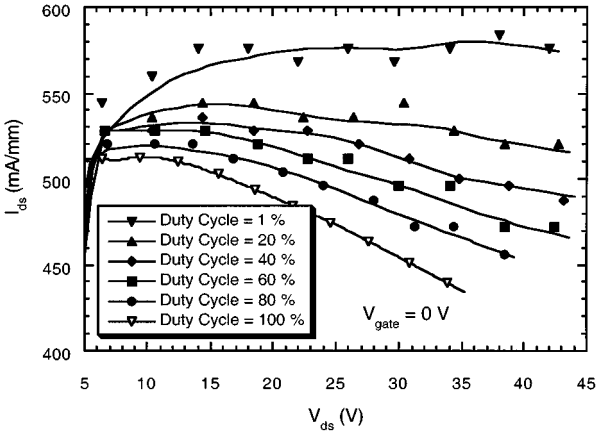


Fig. 4. Drain current for various duty cycles at $V_{\rm GS} = 0$ V at 300 K.

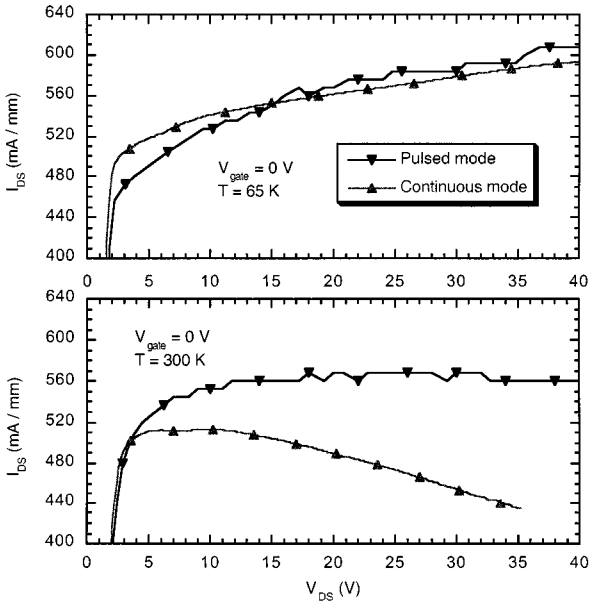


Fig. 5. Drain current at $V_{\rm GS} = 0$ V under pulsed and continuous conditions at $T = 65$ K and $T = 300$ K.

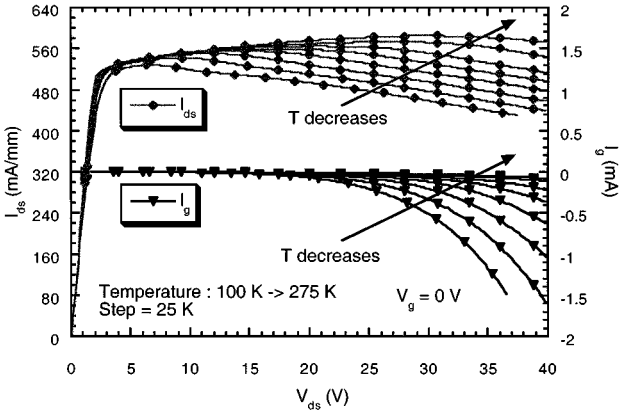


Fig. 6. Drain and gate current for various temperatures at $V_{\rm GS} = 0$ V.

the temperature decreases, the drain voltage threshold increases. This is interpreted as an extension of the drain voltage range for which the DUT does not suffer from self-heating. At the same time, a decrease in the temperature reduces the gate current.

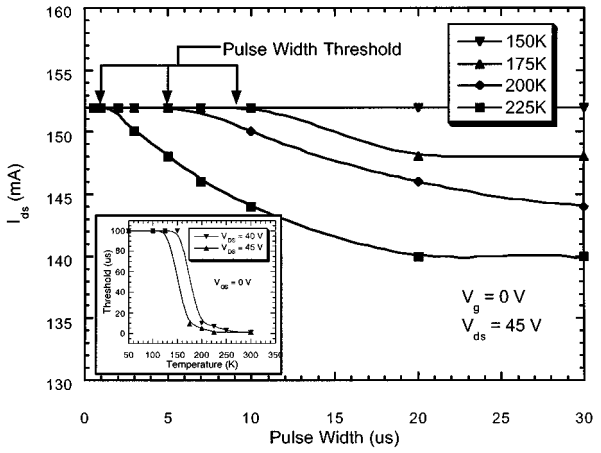


Fig. 7. Drain current versus pulsewidth for pulsewidth threshold determination (isothermal environment) at various temperatures.

At any bias and temperature condition, it is possible to define the pulsewidth threshold as the pulsewidth that leads to a drain current saturation. Fig. 7 displays the pulsewidth threshold for $V_{\rm DS} = 45$ V, $V_{\rm GS} = 0$ V, a period of 100 μs, and at several temperatures. We observe that at 150 K, the drain current is saturated at all available pulsewidths. This is perceived as an absence of any heating effects. Above 225 K, the drain current could not be saturated at any available duty cycle (the minimum duty cycle used was 1%). Therefore, it is possible to say that the pulsewidth threshold is below 1 μs for temperatures greater than 225 K. For temperatures between 150–225 K saturation of the drain current was observed and, thus, a threshold value was extracted. We observed that the threshold value to achieve drain current saturation increases while temperature decreases, meaning that a reduction in the external temperature decreases self-heating effects in the device. Fig. 7 also shows the pulsewidth threshold as a function of temperature for two different bias conditions.

B. Small-Signal RF Characterization

S-parameters allow one to study small-signal device performances. They enable the derivation of the stability factor, cutoff frequency ($f_{\rm T}$), maximum frequency of oscillation ($f_{\rm MAX}$), and load and source stability circles. These extracted parameters help one understand the behavior of devices under a large-signal mode of operation. The load and source contours give initial matching conditions for maximum output power and gain.

$f_{\rm T}$ and $f_{\rm MAX}$ are extracted, respectively, from the short-circuit current gain (h_{21}) and the maximum available unilateral gain ($G_{A,\,\rm Max}$) calculated using the following expressions:

$$h_{21} = \frac{-2 \cdot S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}}$$

$$G_{A,\,\rm Max} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2) \cdot (1 - |S_{22}|^2)}.$$

Fig. 8 shows short-circuit current gain and maximum available gain under different temperature conditions. The cutoff frequency ($f_{\rm T}$) and the maximum frequency of oscillation ($f_{\rm MAX}$) improve while reducing the temperature of operation.

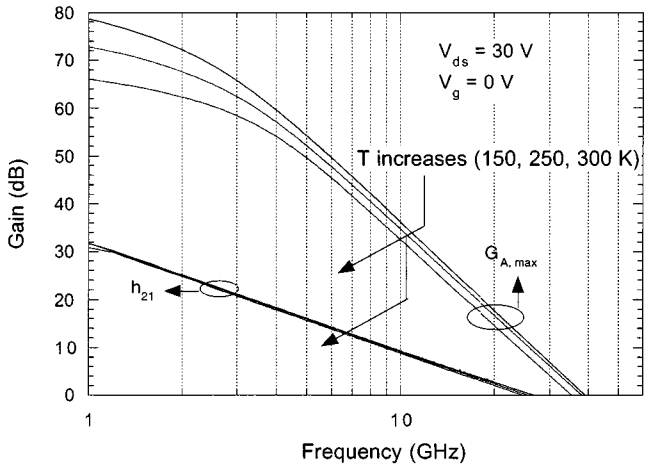


Fig. 8. Short-circuit current gain and maximum available gain at different temperatures (300, 250, 150 K).

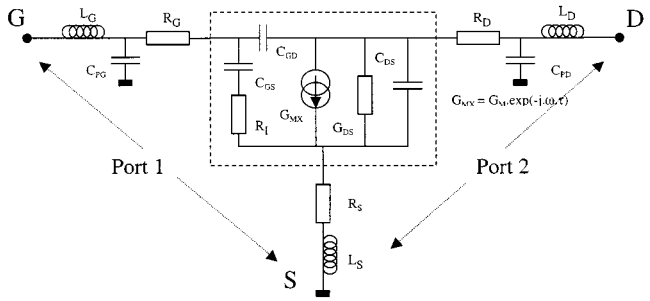


Fig. 9. Equivalent-circuit diagram of an HEMT used for parameter extraction and modeling.

IV. Modeling of GaN HEMT

A standard hybrid-Pi topology is used to simulate the characteristics of a GaN HEMT (Gatewidth $= 125 \times 2$ μm, $L_{\rm GS} = 0.1$ μm, and $L_{\rm GD} = 3$ μm) from 1 to 15 GHz over a complete range of bias conditions and temperatures. As shown in the equivalent circuit (Fig. 9), the value of 15 parameters are determined to simulate the device characteristics under small-signal operations. The elements outside the dotted box represent the extrinsic part of the device. They come from the metal traces and the probing pads [19]. "ColdFET" measurements in conjunction with an improved equivalent circuit based on geometrical considerations of the device lead to the parasitic element values determination. Intrinsic element values are determined analytically from the intrinsic Y-parameters. Finally, a computer-aided design (CAD) tool is used to optimize all parameters values.

A. Extraction of Parasitic Elements

S-parameters measurements at zero drain bias can be used to determine the device extrinsic parameters because the equivalent circuit is much simpler [19], [20].

Parasitic capacitances are obtained from the Y-parameters recorded under pinchoff conditions. The small-signal model presented in this paper simulates a highly nonsymmetric device ($L_{\rm GS} = 0.1$ μm, $L_{\rm GD} = 3$ μm), and equations from Dambrine *et al.* [19] and White *et al.* [20] yield to negative values for the extrinsic capacitances. The equivalent circuit proposed in [19] and [20] under pinchoff conditions considered a uniform repartition of the fringing capacitance C_B under the gate. Two scaling coefficients, based on the geometry of the device, are added to take into account the asymmetry of the device. Fig. 10(a) shows a schematic cross section of the transistor at zero drain bias, showing the physical origin of the scaling coefficients, and Fig. 10(b) presents a complete equivalent circuit under such bias conditions. A gate centered with the drain and source would lead to two equal scaling coefficients and, therefore, to the model proposed by Dambrine *et al.* By neglecting the influence of the inductances and the resistances, the imaginary part of the Y-parameters of the previous circuit are given by

$$\begin{aligned}
{\rm Im}(Y_{11}) &= j.\omega.(C_{\rm PG} + (a+b).C_B) \\
{\rm Im}(Y_{12}) &= {\rm Im}(Y_{21}) = -j.\omega.a.C_B \\
{\rm Im}(Y_{22}) &= j.\omega.(C_{\rm PD} + a.C_B)
\end{aligned}$$

where a and b are the two scaling coefficients. Fig. 11 presents the absolute values of the Y-parameters imaginary part measured at zero drain bias and under pinchoff conditions. The extracted capacitances values are $C_{\rm PD} = 34.6$ fF, and $C_{\rm PG} = 44.22$ fF ($a = 3$ and $b = 0.1$).

Parasitic inductances and resistances are obtained from measurements at zero drain bias and under forward gate-bias conditions [19]. Under such bias conditions, the Z-parameters can be expressed as

$$\begin{aligned}
Z_{11} &= R_S + R_G + \frac{R_C}{3} + \frac{n.k.T}{q.I_G} + j.\omega.(L_S + L_G) \\
Z_{12} &= Z_{21} = R_S + \frac{R_C}{2} + j.\omega.L_S \\
Z_{22} &= R_S + R_D + R_C + j.\omega.(L_S + L_D)
\end{aligned}$$

where R_C represents the channel resistance.

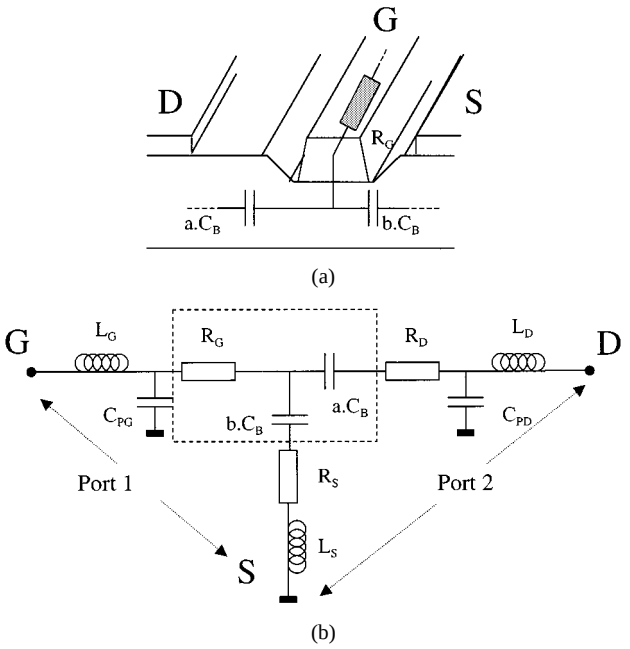


Fig. 10. (a) Schematic cross section of an HEMT at $V_{\rm DS} = 0$ V showing the physical origin of scaling elements for an equivalent circuit under pinchoff conditions. (b) Equivalent circuit of pinchoff FET at $V_{\rm DS} = 0$ V.

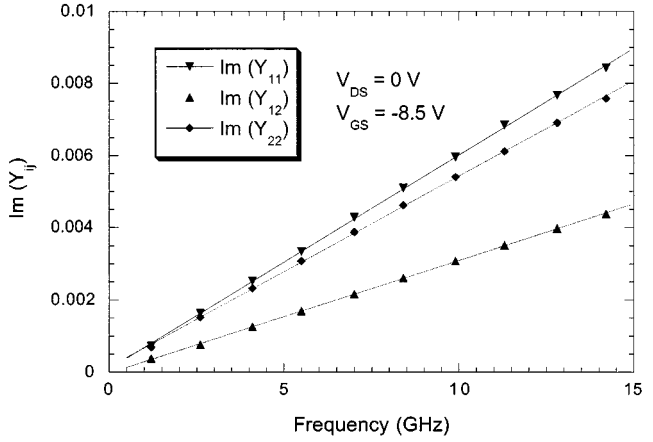


Fig. 11. Imaginary part of Y-parameters versus frequency for an HEMT device biased beyond pinchoff at $V_{\rm DS} = 0$ V for parasitic capacitances determination.

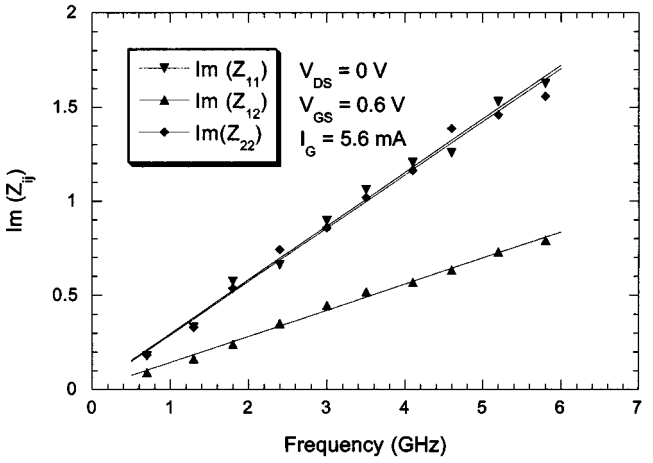


Fig. 12. Imaginary part of Z-parameters versus frequency under forward gate-bias voltage and zero drain-bias voltage for parasitic inductances determination.

The extrinsic inductances can, therefore, be extracted from the imaginary part of the Z-parameters. Fig. 12 shows results derived from S-parameters measurements. The calculated parasitic inductance values are $L_{\rm S} = 22$ pH, $L_{\rm D} = 23.1$ pH, and $L_{\rm G} = 23.4$ pH.

The real parts of Z_{12} and Z_{22} (Fig. 13) lead to two equations involving the parasitic resistances, as well as the channel resistance. A third relation is obtained by knowing the real part of Z_{11} under various gate conditions [see Fig. 14(a) and (b)]. An additional relation required for unequivocal resistance determination can be obtained from various methods [19]. In this model, the parasitic resistances are expressed as a function of the channel resistance (Fig. 15), and a range of possible values for R_C is determined by considering that all resistance values must be kept positive. An initial value for the extrinsic resistances is then determined by taking the channel resistance value in the middle of its range.

B. Extraction of Intrinsic Elements

The intrinsic elements can be analytically determined from the intrinsic Y-parameters [21] obtained after deembedding the parasitic elements from the measured S-parameters through a series of matrix operations [19]. Fig. 16(a) presents the extracted transconductance G_M on a complete bias range at $T = 150$ K and $T = 300$ K. It illustrates the improvement of the GaN HEMT characteristics while operating at reduced

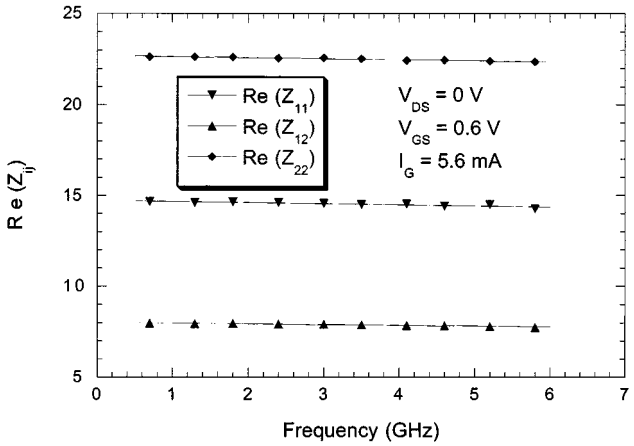
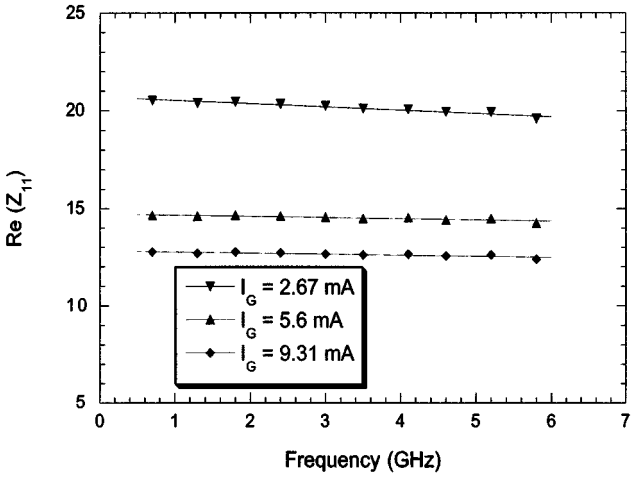
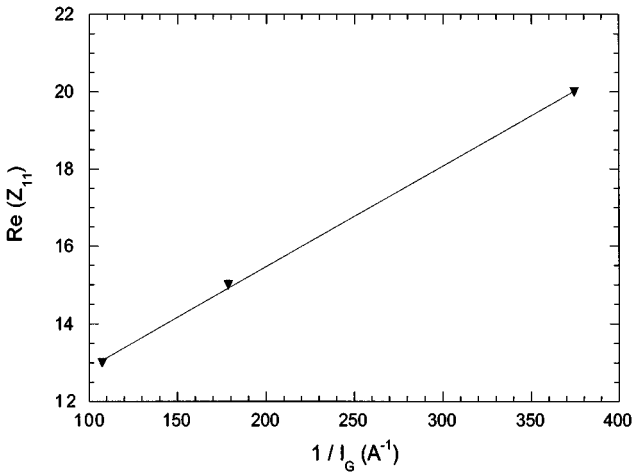


Fig. 13. Real part of Z-parameters versus frequency under forward gate-bias voltage and zero drain-bias voltage for parasitic resistances determination.



(a)



(b)

Fig. 14. (a) Real part of Z_{11} versus frequency under various forward gate-bias voltage and zero drain-bias voltage for parasitic resistances determination. (b) Real part of Z_{11} at zero drain bias versus $1/I_{\rm G}$ for parasitic resistances determination.

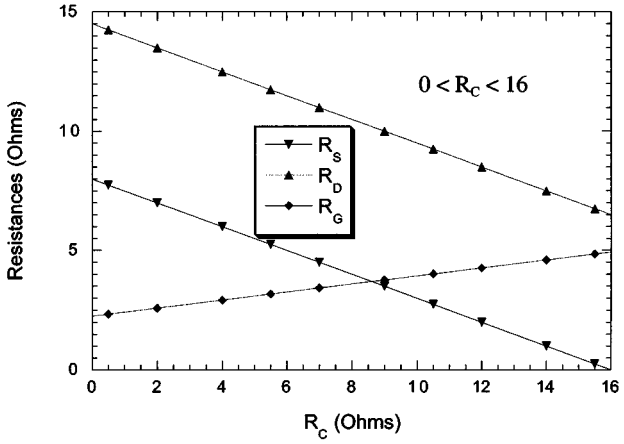
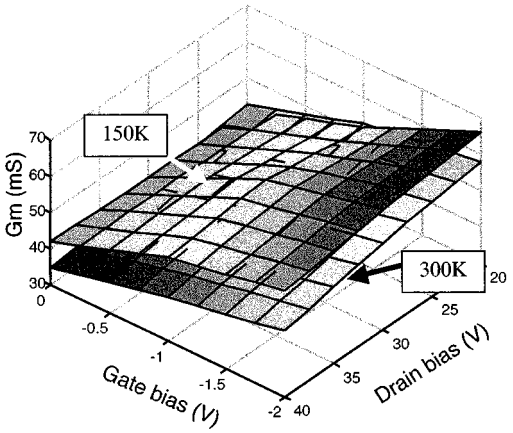


Fig. 15. Parasitic resistances versus channel resistance.



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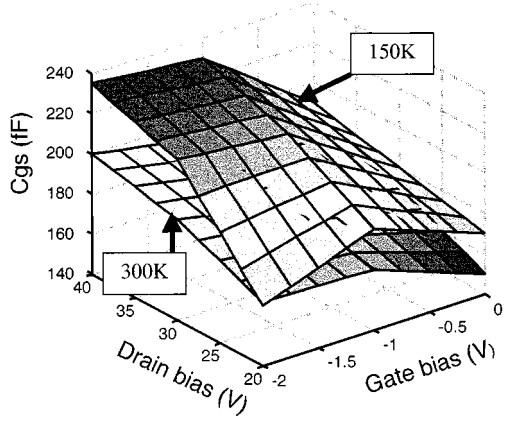


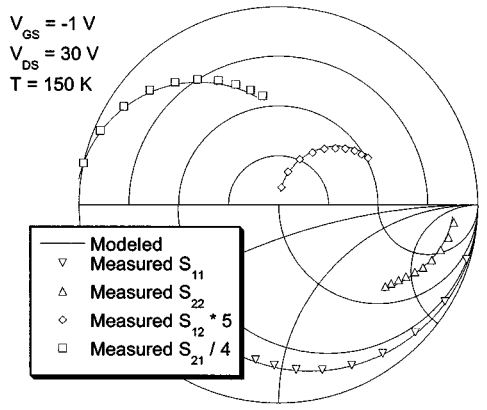
(b)

Fig. 16. (a) Extracted transconductance G_M versus gate and drain bias at $T = 150$ K and $T = 300$ K. (b) Extracted gate-to-source capacitance $C_{\rm GS}$ versus gate and drain bias at $T = 150$ K and $T = 300$ K.

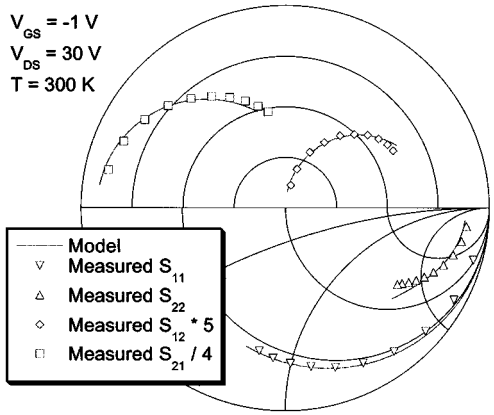
temperature, confirming results obtained from dc–*IV* measurements. Fig. 16(b) shows an increase of the gate-to-source capacitance on a wide bias range when the temperature of operation is reduced from 300 to 150 K.

C. Results

A design tool is used to tune the final value of extrinsic and intrinsic parameters. The extrinsic parameters values are finally



(a)



(b)

Fig. 17. (a) Comparison of measured and modeled S-parameters at $V_{\rm DS} = 30$ V, $V_{\rm GS} = -1$ V, $f = 1$–15 GHz, and $T = 150$ K. (b) Comparison of measured and modeled S-parameters at $V_{\rm DS} = 30$ V, $V_{\rm GS} = -1$ V, $f = 1$–15 GHz, and $T = 300$ K.

TABLE I

	C_{GS}	C_{DS}	C_{GD}	R_I	$1/G_{DS}$	G_M
T = 150K	210 fF	11 fF	21.5 fF	0.1 Ω	588 Ω	57 mS
T = 300K	182 fF	3.5 fF	26 fF	10 Ω	650 Ω	50 mS

$L_{\rm G} = 23.4$ pH, $L_{\rm D} = 23.1$ pH, $L_{\rm S} = 22$ pH, $R_{\rm G} = 3.5\ \Omega$, $R_{\rm D} = 15\ \Omega$, $R_{\rm S} = 5\ \Omega$, $C_{\rm PG} = 36.9$ fF, and $C_{\rm PD} = 27.9$ fF. Small-signal simulations are performed from 1 to 15 GHz at $V_{\rm GS} = -1$ V and $V_{\rm DS} = 30$ V at $T = 150$ K [see Fig. 17(a)] and at $T = 300$ K [see Fig. 17(b)]. Table I summarizes the intrinsic element values at both temperatures.

V. Load–Pull Characterization of GaN HEMTs

As presented earlier, self-heating occurs under large drain bias and at high drain current in a continuous mode of operation. The pulsed load–pull system allows us to measure RF power characteristics of a device under various load and source terminations and under pulsed RF and bias conditions, enabling us to know the power characteristics of power devices in a heat-free mode of operation. We propose here to study the influence of self-heating on RF power characteristics.

Fig. 18 shows the RF power performance into 50-Ω termination of a GaN HEMT sample when operated at reduced lattice temperature. Measurements are achieved under pulsed and

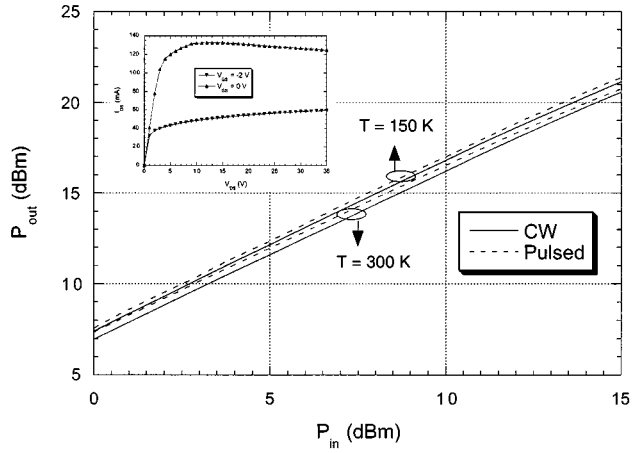


Fig. 18. Output power versus frequency under pulsed and continuous conditions into 50-Ω termination at $T = 150$ K and $T = 300$ K ($V_{\rm DS} = 30$ V, $V_{\rm GS} = 0$ V). The insert shows $I_{\rm DS}(V_{\rm DS})$ data at 300 K, $V_{\rm GS} = 0$ V, and $V_{\rm GS} = -2$ V with $V_{\rm DS}$ up to 35 V.

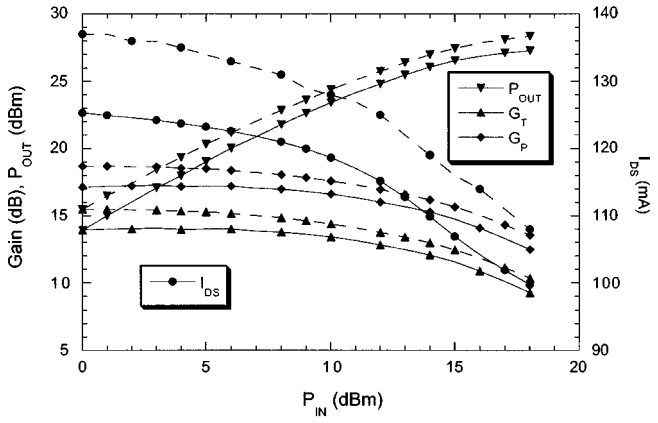


Fig. 19. Pulsed (dashed lines) and continuous (solid lines) RF power measurement results into terminations for maximum output power at $f = 10$ GHz, $V_{\rm DS} = 30$ V, $V_{\rm GS} = 0$ V, and $T = 300$ K.

continuous wave (CW) mode of operation at $V_{\rm GS} = 0$ V and $V_{\rm DS} = 30$ V. As the temperature decreases, the heating effects become less important, resulting in little difference between CW and pulsed RF/bias power measurements. The pulsed power measurements are achieved with a 5-μs pulsewidth on the gate side, a 3-μs pulsewidth for the drain, and a 2-μs pulsewidth for the RF signal ($f = 10$ GHz). While the absence of a negative slope in $I_{\rm DS}(V_{\rm DS})$ at $V_{\rm G} = -2$ V, shown in the inset of Fig. 18, is characteristic of a heat-free environment, the negative output conductance for $V_{\rm DS}$ greater than 12 V at $V_{\rm G} = 0$ V tells us that self-heating is not negligible.

Fig. 19 illustrates the transducer and power gain of the device under both a pulsed and continuous mode of operation tuned for maximum output power at the 1-dB compression point. Optimum load and source impedances were determined under a pulsed condition. The pulsed power measurements are achieved with a 3.4-μs pulsewidth on the gate side, a 3.2-μs pulsewidth for the drain, and a 3-μs pulsewidth for the RF signal ($f = 10$ GHz). The duty cycle was set to 1%. It is the first time that the reflected power is measured under a pulsed condition. The device exhibits an improvement of gain when operating under pulsed conditions. Additionally, Fig. 19 shows the drain-to-source current under a pulsed and continuous regime. As expected, the drain current is larger under a pulsed mode because the device operates in a heat-free regime.

VI. Conclusion

In addition to detailed on-wafer measurements results of dc–*IV*, pulsed-*IV*, and S-parameters, a novel pulsed load–pull system featuring reflected power measurements has been built and utilized to measure, for the first time, RF power characteristics of GaN HEMTs at various temperatures of operation under a pulsed condition. These measurements allow the understanding of self-heating effects in GaN-based transistors and the possibility for device structure improvement resulting in better device performance. The measurement results give an in-depth understanding of the device behavior and are the basis for robust device modeling. A small-signal model that takes into account the device geometry for parasitic extraction has also been developed at different temperatures of operation.

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References

[1] N. Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *IEEE Electron Device Lett.*, vol. 21, Sept. 2000.

[2] E. Gebara, N. Rorsman, J. Olsson, H. Zirath, K. Eklund, and J. Laskar, "Power characteristics of high voltage LDMOS transistors," in *30th Eur. Microwave Conf.*, vol. 3, Paris, France, 2000, pp. 8–11.

[3] S. T. Allen, W. L. Pribble, R. A. Sadler, T. S. Alcorn, Z. Ring, and J. W. Palmour, "Progress in high power SiC microwave MESFETs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, 1999, pp. 321–324.

[4] C. H. Chen, K. Krishnamurthy, S. Keller, G. Parish, M. Rodwell, U. K. Mishra, and Y. F. Wu, "AlGaN/GaN dual-gate modulation-doped field-effect transistors," *Electron. Lett.*, vol. 35, no. 11, pp. 933–935, May 1999.

[5] S. T. Shepard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, "High-power microwave GaN/AlGaN HEMT's on semi-insulating silicon carbide subtrates," *IEEE Electron Device Lett.*, vol. 20, pp. 161–163, Apr. 1999.

[6] E. Gebara, D. Heo, J. Laskar, and M. Harris, "Development of temperature dependent load–pull analysis techniques," in *Proc. GaAs 1999*, Munich, Germany, pp. 286–290.

[7] G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. L. Pierson, and B. T. McDermott, "High-power 10-GHz operation of AlGaN HFET's on insulating SiC," *IEEE Electron Device Lett.*, vol. 19, pp. 198–200, June 1998.

[8] J. M. Collantes, Z. Ouarch, C. Y. Chi, M. Sayed, and R. Quere, "Discrepancies obtained in transconductance extracted from pulsed-*IV* curves and from pulsed S-parameters in HEMT's and PHEMTs," *Electron. Lett.*, vol. 34, no. 3, pp. 291–292, Feb. 1998.

[9] M. Paggi, P. H. Williams, and J. M. Borrego, "Nonlinear GaAs MESFET modeling using pulsed gate measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1593–1597, Dec. 1998.

[10] J. F. Vidalou, F. Grossier, M. Camiade, and J. Obregon, "On-wafer large signal pulsed measurements," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1989, pp. 831–834.

[11] D. Heo, E. Gebara, Y. E. Chen, S. Yoo, M. Hamai, Y. Suh, and J. Laskar, "An improved deep submicrometer MOSFET RF nonlinear model with new breakdown current model and drain-to-substrate nonlinear coupling," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2361–2369, Dec. 2000.

[12] S. H. Song, D. M. Kim, H. J. Kim, S. H. Kim, K. N. Kang, and M.I. Nathan, "Photonic microwave characteristics and modeling of an $Al_{0.3}/Ga_{0.7}/As/GaAs/In_{0.13}/Ga_{0.87}/As$ double heterostructure pseudomorphic HEMT," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 35–37, Jan. 1998.

[13] M. Liang and M. E. Law, "Influence of lattice self-heating and hot-carrier transport on device performance," *IEEE Trans. Electron Devices*, vol. 41, pp. 2391–2398, Dec. 1994.
[14] S. Prichett, R. Stewart, J. Mason, and G. Brehm, "Precision pulsed I–V system for accurate GaAs device I–V plane characterization," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1994, pp. 1353–1356.
[15] J. M. Collantes, Z. Ouarch, C. Y. Chi, M. Sayed, and R. Quere, "Discrepancies obtained In transconductance Extracted from pulsed-IV curves and from pulsed S-parameters in HEMT's and PHEMTs," *Electron. Lett.*, vol. 34, no. 3, pp. 291–292, Feb. 1998.
[16] J. Rodriguez-Tellez, "Behavior of GaAs FET pulsed IV characteristics," *Microwave J.*, pp. 332–335, May 1998.
[17] U. K. Mishra, Y. F. Wu, B. P. Keller, and S. P. Denbaars, "GaN microwave electronics," in *Proc. Topical Millimeter Waves Symp.*, 1997, pp. ???–???.
[18] M. Paggi, P. H. Williams, and J. M. Borrego, "Nonlinear GaAs MESFET modeling using pulsed gate measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1593–1597, Dec. 1988.
[19] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1160, July 1988.
[20] P. White and R. Healy, "Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from 'ColdFET' measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 3, pp. 453–455, July 1993.
[21] M. Berroth and R. Bosh, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 891–895, July 1990.

Sebastien Nuttinck received the Engineering Diploma in physics from the National Institute of Applied Sciences in Toulouse, Toulouse, France, in 1999, the Master degree in microelectronics (with highest honors) from the Paul Sabatier University, Toulouse, France, in 1999, and is currently working toward the Ph.D. degree in electrical engineering at the Georgia Institute of Technology, Atlanta.

He is currently with the Microwave Application Group, School of Electrical Engineering, Georgia Institute of Technology. His research interests are the characterization and the modeling of high-power devices (e.g., GaN, etc.).

Edward Gebara received the B.S. degree in electrical engineering (with highest honor) and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 1996 and 1999, respectively, and is currently working toward the Ph.D. degree at the Georgia Institute of Technology.

He is currently with Quellan Inc., Atlanta, GA, where he is involved with the development of new technology for next-generation optical links. His main research interest involves device characterization, large- and small-signal active device modeling, and monolithic-microwave integrated-circuit (MMIC) designs.

Joy Laskar (S'84–M'85) received the B.S. degree in computer engineering (with highest honors) from Clemson University, Clemson, SC, in 1985, and the M.S. and the Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign, in 1989 and 1991, respectively.

He has held faculty positions at the University of Illinois and the University of Hawaii. In 1995, he joined the Georgia Institute of Technology, Atlanta, where he is currently the Chair for the Electronic Design and Applications Technical Interest Group, the Director of Research for the State of Georgia's Yamacraw Initiative, and the National Science Foundation (NSF) Packaging Research Center System Research Leader for RF and Wireless. He also heads a research group of 25 members at the Georgia Institute of Technology with a focus on integration of high-frequency electronics with optoelectronics and integration of mixed technologies for next-generation wireless and opto-electronic systems. He has authored or co-authored over 100 papers, numerous invited talks, and has ten patents pending. His research has focused on high-frequency integrated-circuit (IC) design and their integration. His research has been supported by over 15 companies and numerous federal agencies including the Defense Advanced Research Projects Agency (DARPA), the National Aeronautics and Space Administration (NASA), and the National Science Foundation (NSF). He is the co-founder of the Broadband Wireless Company RF Solutions and co-founder of the next-generation optical technology company Quellan Inc.

Dr. Laskar is a co-organizer and chair for the Advanced Heterostructure Workshop, serves on the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Symposia Technical Program Committee, and is a member of the North American Manufacturing Initiative Roadmapping Committee. He was the 1995 recipient of the Army Research Office's Young Investigator Award, the 1996 recipient of the NSF's CAREER Award, the 1997 NSF Packaging Research Center Faculty of the Year, the 1998 NSF Packaging Research Center Educator of the Year, the 1999 IEEE Rappaport Award (Best IEEE Electron Devices Society Journal Paper), the 2000 corecipient of the IEEE MTT-S International Microwave Symposium (IMS) Best Paper award, and the 2001 Georgia Tech Faculty Graduate Student Mentor of the Year.

Herbert M. Harris (S'73–M'74–SM'98) received the B.Sc. and M.Sc. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1974 and 1980, respectively.

From 1974 to 1976, he was with Harris Semiconductor, Melbourne, FL where he served as a Senior Reliability Engineer on digital CMOS circuits and bipolar memory products. In 1976, he joined the Georgia Institute of Technology Research Institute, Atlanta, GA, as a Research Engineer. He is currently a Principal Research Engineer and Division Chief in the Electro-Optics, Environment, and Materials Laboratory, Georgia Institute of Technology Research Institute, where he manages a staff of engineers and scientists who perform research in semiconductor materials, devices and circuits, and integrated optic components for chemical sensing applications.

Mr. Harris is a Registered Professional Engineer in the State of Georgia.